EXHIBIT “A”

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90/019,426	02/21/2024	6816809	G0930.70003US00	2089

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/019,426* .

PATENT UNDER REEXAMINATION *6816809* .

ART UNIT *3992* .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Order Granting Request For Ex Parte Reexamination	**Control No.** 90/019,426	**Patent Under Reexamination** 6816809	
	Examiner DENNIS G BONSHOCK	**Art Unit** 3992	**AIA (FITF) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed 02/21/2024 has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☑ PTO/SB/08, c)☐ Other: ____

1. ☑ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

cc:Requester (if third party requester)

DECISION ON REQUEST FOR REEXAMINATION

A substantial new question (SNQ) of patentability affecting claims 1-17 of United States Patent Number: 6,816,809 issued to Circenis (hereinafter the '809 Patent) is raised by the Request for *ex parte* reexamination filed 2/21/2024. Since the Requester did not request reexamination of claims 18-20 of the '809 Patent, nor present a Substantial New Question of Patentability (SNQ) for said claims, claims 18-20 will not be reexamined.

The Office's determination in both the order for reexamination and the examination stage of the reexamination ordered will generally be limited solely to a review of the claim(s) for which reexamination was requested (see: MPEP 2240 & 2243). Additionally, if a Requester fails to set forth the pertinency and manner of applying the cited art to a claim as required by 37 CFR 1.510(b), that claim will generally not be reexamined. This matter was squarely addressed in *Sony Computer Entertainment America Inc. v. Dudas*, 85 USPQ2d 1594 (E.D. Va 2006). The District Court upheld the Office's discretion to not reexamine claims in an *Inter Partes* Reexamination proceeding other than those claims for which reexamination had specifically been requested.

Information Disclosure Statement

Regarding Information Disclosure Statement (IDS) submissions, MPEP 2256 recites the following: "Where patents, publications, and other such items of information are submitted by a party (patent owner or requester) in compliance with the requirements of the rules, the requisite degree of consideration to be given to such information will be normally limited by the degree to which the party filing the information citation has explained the content and relevance of the information. The initials of the examiner placed adjacent to the citations on the form PTO/SB/08A and 08B or its equivalent, without an indication to the contrary in the record, do not signify that the information has been considered by the examiner any further than to the extent noted above."

Accordingly, the IDS submission filed by Third Party Requester (3PR) on 2/21/2024 has been considered by the Examiner only with the scope required by MPEP 2256, unless otherwise noted.

References

The Request presents that the following references as providing relevant teachings with regard to claims 1-17 of the '809 Patent:

- M.M. Theimer and K.A. Lantz, "Finding Idle Machines in a Workstation-based Distributed System," EEE Transactions on Software Engineering, vol. 15, no. 11, pp. 1444-1458 (November 1989) (EX1101, "Theimer')
- Japanese Patent Application No. 60-24655 (EX1005, "Ogawa'")

- E. Hoekstra et al., "Design and Implementation of a DSP Based MPEG-1 Audio Encoder," JEEE Transactions on Consumer Electronics, vol. 45, no. 1, pp. 31-35 (Oct. 1998) (EX1102, "Hoekstra"')
- U.S. Patent No. 7,032,119 (EX1103, "Fung-119")
- U.S. Patent No. 6,166,984 (EX1007, "Bohac'")
- U.S. Patent No. 4,458,307 (EX1010, "McAnlis'")
- U.S. Patent Pub. No. 2002/0133728 (EX1104, "Agarwal')

Affidavits, Declaration, or Other Written Evidence

The Examiner recognizes that a declaration by Vijay K. Madisetti, PH.D. Under 37 C.F.R. § 1.132 (executed on 2/21/2024) has been referenced in support of Third Party Requester. The declaration (hereafter the "Madisetti Declaration" or "Madisetti") has been considered and made of record.

The Examiner further notes that affidavits or declarations or other written evidence which explain the contents or pertinent dates of prior art patents or printed publications in more detail may be considered in reexamination (see: MPEP 2258(I)(E)), but any rejection must be based upon the prior art patents or printed publications as explained by the affidavits or declarations or other written evidence. The rejection in such circumstances cannot be based on the affidavits or declarations or other written evidence as such, but must be based on the prior art patents or printed publications.

Prosecution History

Original Examination:

The '809 Patent was originally filed as U.S. Patent Application Serial No. 10/200,175 on July 23, 2002.

On 10/6/2003, the Office mailed a Non-Final rejection in which the claims were rejected under 35 USC § 103 over U.S. Patent No: 6,049,798 (to "Bishop") and U.S. Patent No.: 4,503,495 (to "Boudreau").

On 1/6/2004, Patent Owner (then Applicant) filed an amendment to the claims further specify a "idle indicator" rather than the previously claimed "state indicator":

1. (Currently Amended) A hardware based utilization metering device, comprising:

[a state] an idle indicator coupled to a processor, wherein the [state] idle indicator receives an indication when the processor is in a first state;

a counter coupled to the [state] idle indicator and coupled to a system clock, wherein the counter receives a measure of system time from the system clock and receives data related to the indication when the processor is in the first state, and generates a counter value indicative of time the processor is in the first state; and

a data usage provider coupled to the counter, wherein the data usage provider is capable of providing the counter value.

On 1/8/2004, the Office conducted an interview between Hien X. Vo (the Examiner of record) and John Harrop (the Attorney of record) where the Examiner noted in his Interview Summary that "Upon a receipt of amendment, the prior arts do not disclose a plurality of processors and the idle indicator of processors in a busy state."

On 4/6/2004, the Office mailed a Notice of Allowance without any further reasons for allowance.

Continuation Application (10/892,231):

The applicant filed U.S. Application No. 10/892,231 ("the '231 application") on July 16, 2004, as a continuation of the '175 application that issued as the '809 patent.

The Examiner for the '231 application was the same Examiner who reviewed the '175 application. The Examiner rejected '231 application claim 1 as anticipated by Vea (EX1006), finding that "Vea discloses... an idle indicator coupled to a processor" and a "counter... coupled to said idle indicator[.]" EX1014, 300. The Examiner also rejected '231 application claim 1 for non- statutory obviousness-type double patenting, finding it "not patentably distinct" from '809 Patent claim 1. EX1014, 296-297. Thus, the Examiner found that Vea anticipated a claim that was patentably indistinct from '809 Patent claim 1.

Following claim amendment, the Examiner rejected amended application claim 1 to "a device for metering processor utilization" as obvious over Vea and another

reference, finding that Vea taught a system clock "to provide a count corresponding to the amount of time spent in at least one of said busy[] and idle states" as well as an "idle indicator" and "a counter" coupled to the idle indicator. EX1014, 366-367.

IPR2022-01197:

On 7/5/2022, Google (the same 3PR as in the present reexam) filed a petition for inter partes review challenging claims 1-17 of the '809 patent in IPR2022-01197 on the following grounds:

Grounds 1-5 relied on Ogawa. EX1107, 10-41.

Grounds 6-8 relied on Vea. EX1107, 41-68.

On 1/3/2023, the Board denied institution. Paper 9, 12-20 (Mar. 29, 2023), attached as EX1108 for the following reasons:

For Grounds 1-5, reviewing the prosecution history, the Board described the Examiner as allowing the claims over Bishop because Bishop disclosed "calculating CPU utilization by, infer alia, running a program on a CPU." EX1108, Paper 9, 17-18. The Board found that "similar to Bishop's device, Ogawa runs a 'program' in order to obtain the CPU's usage rate." EX1108, Paper 9, 18. The Board found that the Petition "has not explained how Ogawa's reliance on a software program to obtain CPU usage is distinguishable over Bishop's use of a software program to calculate CPU activity, or demonstrated sufficiently how such reliance on software corresponds to the limitations in claim 1." EX1108, Paper 9, 19.

For Grounds 6-8, the Board denied institution in its discretion under 35 U.S.C. §325(d), as a European counterpart to Vea was shown to be evaluated after allowance, by the Examiner initialing next to it on a 1449.

Litigation History

The '809 Patent has been involved in the following litigation (currently STAYED pending resolution of IPR petitions on five of six asserted patents including the '809 patent):

Valtrus Innovations, Ltd. v. Google LLC, No. 3:22-cv-00066-N (N.D. Tex.)

Substantial New Question of Patentability

The presence or absence of "a substantial new question of patentability" determines whether or not reexamination is ordered. For a substantial new question of patentability to be present, it is only necessary that: (A) the prior art patents and/or printed publications raise a substantial question of patentability regarding at least one claim, i.e., the teaching of the (prior art) patens and printed publications is such that a reasonable examiner would consider the teaching to be important in deciding whether or not the claim is patentable; and (B) the same question of patentability as to the claim has not been decided by the Office in an earlier concluded examination or review of the patent, raised to or by the Office in a pending reexamination or supplemental

examination of the patent, or decided in a final holding of invalidity (after all appeals) by a federal court in a decision on the merits involving the claim. If a reexamination proceeding was terminated/vacated without resolving the substantial question of patentability question, it can be re-presented in a new reexamination request. It is not necessary that a "prima facie" case of unpatentability exist as to the claim in order for a substantial new question of patentability to be present as to the claim. Thus, a substantial new question of patentability as to a patent claim could be present even if the examiner would not necessarily reject the claim as either fully anticipated by, or obvious in view of, the prior art patents or printed publications (see: MPEP 2242(I)).

In a decision to order reexamination made on or after November 2, 2002, reliance on old art does not necessarily preclude the existence of a substantial new question of patentability that is based exclusively on that old art. See Public Law 107-273, 116 Stat. 1758, 1899-1906 (2002), which expanded the scope of what qualifies for a substantial new question of patentability upon which a reexamination may be based. Determinations on whether a substantial new question of patentability exists in such an instance shall be based upon a fact-specific inquiry done on a case-by-case basis. For example, a substantial new question of patentability may be based solely on old art where the old art is being presented/viewed in a new light, or in a different way, as compared with its use in the earlier examination(s), in view of a material new argument or interpretation presented in the request. Such material new argument or interpretation may be based solely on claim scope of the patent being reexamined (see: MPEP 2242(II)(A)).

Claim 1 is presented below with underlined text showing the limitations that are believed to be the critical limitations, given the prosecution history recited above, and which are used by the Examiner to show how specific teachings of the proposed references raise a substantial new question of patentability.

1. A hardware based utilization metering device, comprising:

an idle indicator coupled to a processor, wherein the idle indicator receives an indication when the processor is in a first state;

a counter coupled to the idle indicator and coupled to a system clock, wherein the counter receives a measure of system time from the system clock and receives data related to the indication when the processor is in the first state, and generates a counter value indicative of time the processor is in the first state; and

a data usage provider coupled to the counter, wherein the data usage provider is capable of providing the counter value.

In the 2/21/2021 Request, the 3PR (Requester) suggests that the following combination of references provide elements which are allegedly equivalent to claims 1-17 of the '809 Patent:

Theimer in view of Ogawa

Proposed Grounds 1 - 3: Claims 1, 2, 5, 6, 9-11, 13-15, and 17 over Theimer in view of Ogawa (in further view of Bohac / McAnlis for several dependent claims)

The Requester alleges that the Theimer reference when combined with Ogawa raises a substantial new question of patentability with respect to claim 1 of the '809 patent. Reading of the Theimer reference on the claims is provided on pages 20-50 of the Request. The proposed rejection further relies AAPA from column 4, lines 35-60 of the '809 patent and noted on pages 16-19 of the Request.

The Theimer reference is new art that provides new, non-cumulative technological teachings that were not previously considered nor discussed on the record during prosecution of the '809 patent.

Ogawa was utilized in IPR, as discussed above, however Ogawa is now being viewed in combination with the Theimer reference, thus being presented in a new light. The above substantial new question of patentability includes a reliance on Ogawa to make up a portion of a proposed rejection, and while Ogawa is still being relied upon for many of the same features, the CPU running a program, of Ogawa, is now being replaced with a CPU advertising its own load information, of Theimer.

With regard to the limitation of a ***hardware based utilization metering device, comprising: an idle indicator coupled to a processor, wherein the idle indicator receives an indication when the processor is in a first state,*** Theimer teaches a system for "Finding Idle Machines in a Workstation-based Distributed System", similar to that of Ogawa, though rather than running a program on the CPU to present its idle status, Theimer presents that the machines periodically advertise their loads to the managing devices (see page 114). While Theimer is not specific on the details of advertising its usage, we know from Applicant's Admitted Prior Art (AAPA) that *"some CPUs include a pin on the CPU chip that provides a halt (idle) indication. Some operating system halt the CPU when the CPU is not processing commands (i.e., the CPU is idle), and a halt (idle) indication (i.e., a high or low, or 0 or 1, value) may be asserted at the pin."… or alternately "the operating system may place ethe CPU into an idle look, where the CPU remains until the operating system requires CPU processing."* (see 4:36-60 of the '809 patent)

"A hardware based utilization metering device:"

Ogawa's Figure 1 "device for measuring a [CPU's] usage rate" (Ogawa, 325) is a hardware-based utilization metering device. Ogawa, 326 (LR) ("arithmetic circuit 8 calculates the usage rate" of CPU 1 based on the CPU's "effective processing time" and "idle time"); Ogawa, 327 (calculates "the usage rate of the [CPU] 1 at a hardware level.").

In Theimer+Ogawa, the workstation processor indicates it is busy by asserting a logical signal on a pin (supra). The workstation CPU is busy when it is performing

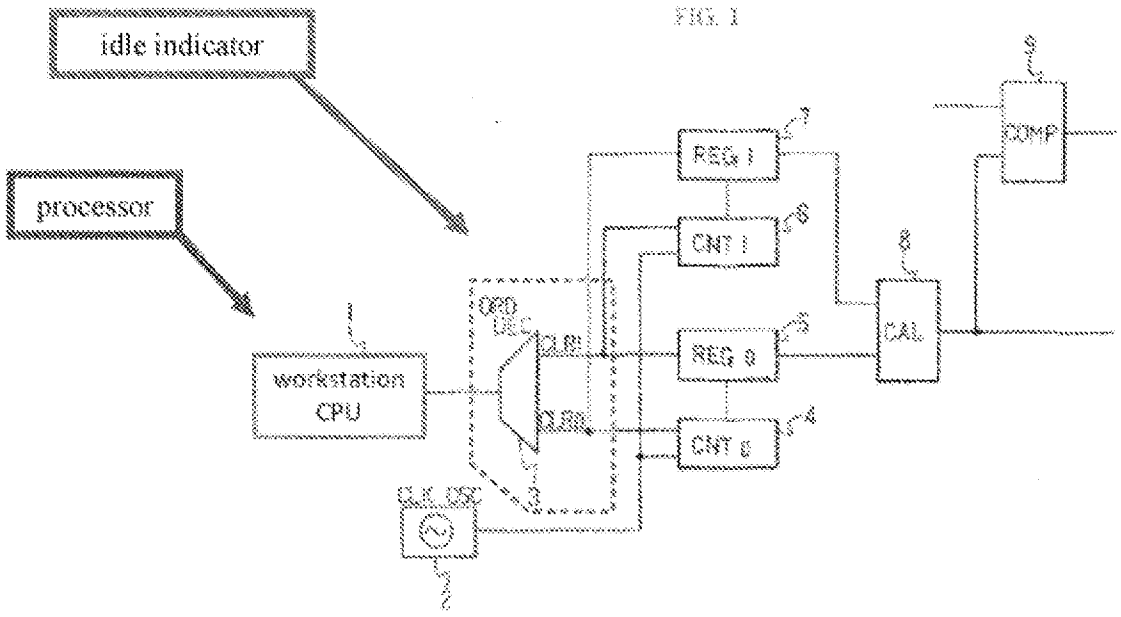
"effective processing" and not busy when it is not. See e.g., Ogawa, 326(UL)-(UR) (the CPU has "effective processing time and idle time"); Theimer explains that "many workstations are completely idle[.]" Theimer, 114.

Theimer+Ogawa provides a "hardware based" device because Theimer's workstation CPU asserts a state indication as a logical signal on a pin exactly like embodiments in the '809 patent (supra), and Ogawa uses logic circuits and other hardware components to measure CPU utilization (supra).

[1A] "idle indicator coupled to a processor, wherein the idle indicator receives an indication when the processor is in a first state"

The '809 patent (3:18-27) describes two processor "states": (1) a "busy" state where "the CPU is running processes that perform useful work for the user," and (2) and an idle state where "the CPU is not performing useful work."

Theimer+Ogawa meets limitation [1A] because Ogawa's modified decoder 3 is "coupled to a processor" and meets [1A]'s idle indicator. Ogawa, Figure 1, 326(UR)-(LL) (CPU 1 is "connected" to counters/registers 4-7 "via the control order decoder 3."). In Theimer+Ogawa, the processor is met by the CPU of each workstation participating in Theimer's scheduling system, rather than Ogawa's "CPU 1" and Ogawa's circuit determines each workstation CPU's utilization (supra).



Theimer+Ogawa in modified / annotated Ogawa Fig. 1.

Modified decoder 3 "receives an indication when the processor is in a first state" in the form of the logic signal asserted, when the processor is in a first state, on the pin connecting the workstation CPU to an Ogawa order decoder 3, meeting limitation [1A] in at least two ways based on the "first" state being either the busy or not-busy (idle) state.

In Theimer+Ogawa, Ogawa's modified encoder receives a signal that has a binary value that indicates when the CPU is in the busy state and when it is in the not busy (idle) state. Thus, Theimer+Ogawa meets limitation [1A] with the first state comprising a "busy" state when the logical signal asserted on the idle pin is high, and also meets limitation [1A] with the first state comprising an "idle" state when the logical signal asserted on the idle pin is low.

Thus, Theimer+Ogawa provides a "first state" for the first state being a busy state as well as the first state being an idle state. Each case separately meets limitation [1A].

It is agreed that the Theimer reference when combined with Ogawa reference does raise a substantial new question of patentability, as proposed in the request, to at least claim 1 of the ‘809 patent. There is a substantial likelihood that a reasonable Examiner would consider these teachings important in deciding whether or not this claim is patentable.

Accordingly, the Theimer reference when combined with Ogawa reference does raise a substantial new question to at least claim 1, which question has not been decided in a previous examination of the ‘809 patent nor was there a final holding of invalidity by the Federal Courts regarding the ‘809 patent.

Neither the Bohac reference nor the McAnlis reference alone raise an SNQ, however when viewed in combination with the Theimer and Ogawa references do raise and SNQ with respect to the following claims: Bohac for claims 6 and 14 and McAnlis for claim 11. Both Bohac and McAnlis are new art that provide new, non-cumulative technological teachings that were not previously considered nor discussed on the record during prosecution of the ‘809 patent.

Hoekstra in view of Ogawa

Proposed Grounds 4 - 6: Claims 1, 2, 5, 6, 9-11, 13-15, and 17 over Hoekstra in view of Ogawa (in further view of Bohac / McAnlis for several dependent claims)

The Requester alleges that the Hoekstra reference when combined with Ogawa raises a substantial new question of patentability with respect to claim 1 of the '809 patent. Reading of the Hoekstra reference on the claims is provided on pages 50-78 of the Request.

The Hoekstra reference is new art that provides new, non-cumulative technological teachings that were not previously considered nor discussed on the record during prosecution of the '809 patent.

Ogawa was utilized in IPR, as discussed above, however Ogawa is now being viewed in combination with the Hoekstra reference, thus being presented in a new light. The above substantial new question of patentability includes a reliance on Ogawa to make up a portion of a proposed rejection, and while Ogawa is still being relied upon for many of the same features, the CPU (running a program) of Ogawa, is now being replaced with the Digital Signal Processor (DSP) algorithm, of Hoekstra.

With regard to the limitation of **a *hardware based utilization metering device, comprising: an idle indicator coupled to a processor, wherein the idle indicator receives an indication when the processor is in a first state***, Hoekstra teaches a system for evaluating processor idle time, similar to that of Ogawa, and also uses code execution on the DSP to assert a logical signal (e.g., low or "0") on the DSP output pin when the DSP was idle…" (see pages 32 and 34 of Hoekstra and page 51 of the request). For similar reasons both Ogawa (in the IPR) and Bishop (in the '175 application) were determined to not read on the claims, specifically, for calculating CPU utilization by, "running a program on a CPU." EX1108, Paper 9, 17-18.

Given that Hoekstra is deficient for the same reasons that both Ogawa and Bishop were previously shown to be deficient for, in supporting 'hardware based utilization metering', it is determined that the combination of Hoekstra and Ogawa does NOT raise a substantial new question of patentability for the reasons set forth above.

Neither the Bohac reference nor the McAnlis reference cure the deficiencies noted above with respect to the Hoekstra and Ogawa references, and therefor don't alone nor in combination with the Hoekstra and Ogawa references raise an SNQ.

Fung-119

Proposed Grounds 7 - 10: Claims 1-17 over Fung-119 alone and in combination with Bohac and Agarwal

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The Requester alleges that the Fung-119 reference raises a substantial new question of patentability with respect to claim 1 of the '809 patent. Reading of the Fung-119 reference on the claims is provided on pages 74-125 of the Request. Fung-119 incorporates by reference U.S. Patent No: 5,710,929, herein referred to as Fung-929.

The Fung-119 reference is new art that provides new, non-cumulative technological teachings that were not previously considered nor discussed on the record during prosecution of the '809 patent.

With regard to the limitation of a ***hardware based utilization metering device, comprising: an idle indicator coupled to a processor, wherein the idle indicator receives an indication when the processor is in a first state,*** Fung is shown to teach:

"A hardware based utilization metering device:"

Fung-929's "hardware monitor 79 monitors the CPU to detect activity and inactivity. The hardware monitor 79 typically is circuitry for detecting inactivity independently from the software and the software monitor 80." Fung-929, 5:44-47. That

is consistent with Fung-929's explanation that "hardware monitor 79 and power management unit 15 are provided in FIG. 3 as a hardware embodiment" Fung-929, 7:1-2.

Fung-929 further teaches, in 5:47-54, that "[H]ardware monitor 79 senses predetermined address ranges, such as an I/O address range and a video memory address range, and monitors the activity of addresses by the CPU to addresses within these ranges. If no data transfers occur within the specified address ranges for predetermined periods of time, then a power control mode is entered to conserve power in the computer system."

Hardware monitor 79 senses these "predetermined address ranges" using activity monitor 16 to evaluate activity on CPU bus 5. Fung-929, Fig. 2, 6:21-24 ("The hardware monitor 79 (using activity monitor 16) analyzes the address activity on the system bus 5 [e.g., CPU bus 5 (Fung-929, 4:38)] to provide activity information used to control power management."), 6:55-58 ([T]he power management unit 15 includes the hardware monitor 79 (activity monitor 16 and timer unit 24) which is designed to operate with minimal system requirements and without software support.").

Annotated Fung-929 Fig. 2 shows hardware monitor 79 comprising activity monitor 16 (AM 16) and timer unit 24 (TV 24) (Fung-929, 6:16-19):

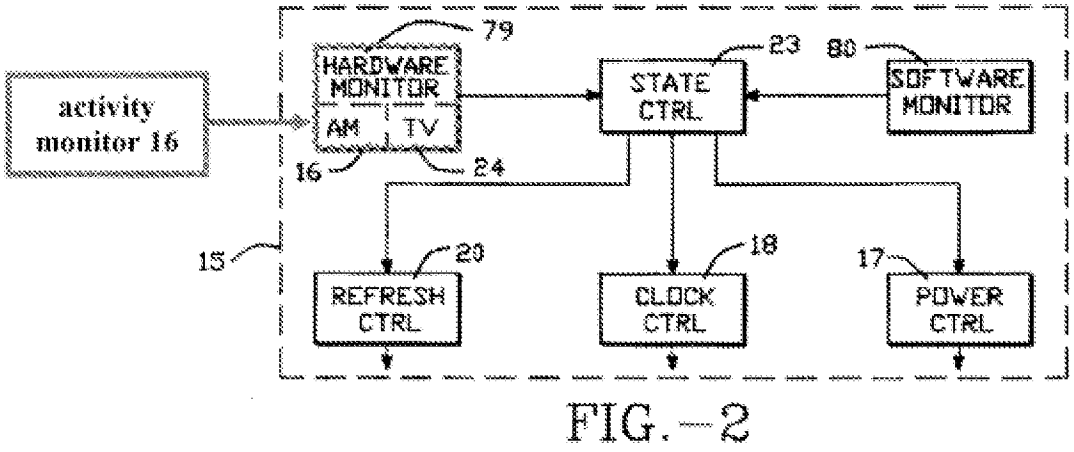


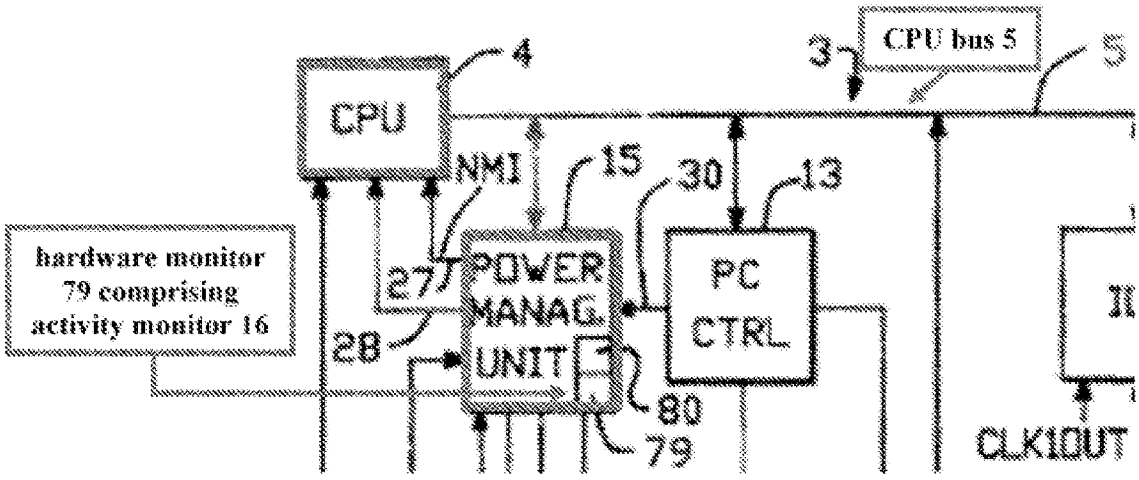
FIG.—2

Fung-929, Fig. 2 (annotated) showing PMU 15 components.

Like hardware monitor 79, activity monitor 16 is hardware. Fung-929, 7:1-2. It "monitors the activity level of the computer system and generates a first inactivity indicator after a first predetermined period of inactivity and a second inactivity indicator a second predetermined period of inactivity after generating the first inactivity indicator." Fung-929, 38:47-54.

(a) "an idle indicator coupled to a processor" (the activity monitor 16)

Activity monitor 16 is coupled to the processor (CPU 4) via CPU bus 5 (Fung-929, 4:35-40). Figure 1 shows power management unit ("PMU") 15 coupled to CPU bus 5. PMU 15 contains hardware monitor 79 which in turn contains activity monitor 16. Fung-929, Fig. 1 (power management unit 15 comprising hardware monitor 79 coupled to CPU 4 and CPU bus 5), Fig. 2 (hardware monitor 79 contains activity monitor 16).



Fung-929, Fig. 1 (annotated, exploded).

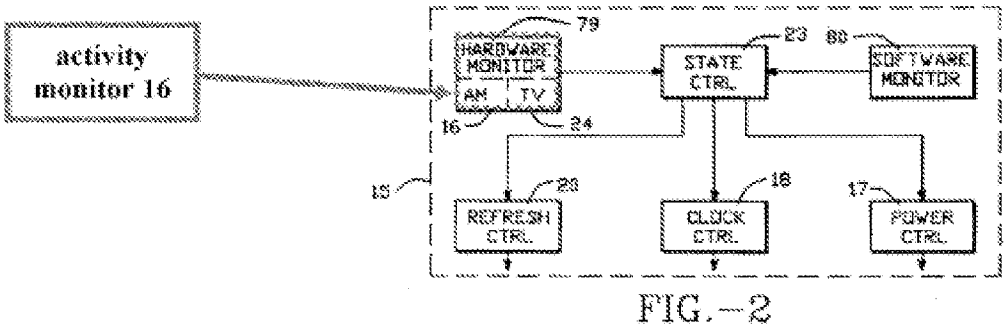
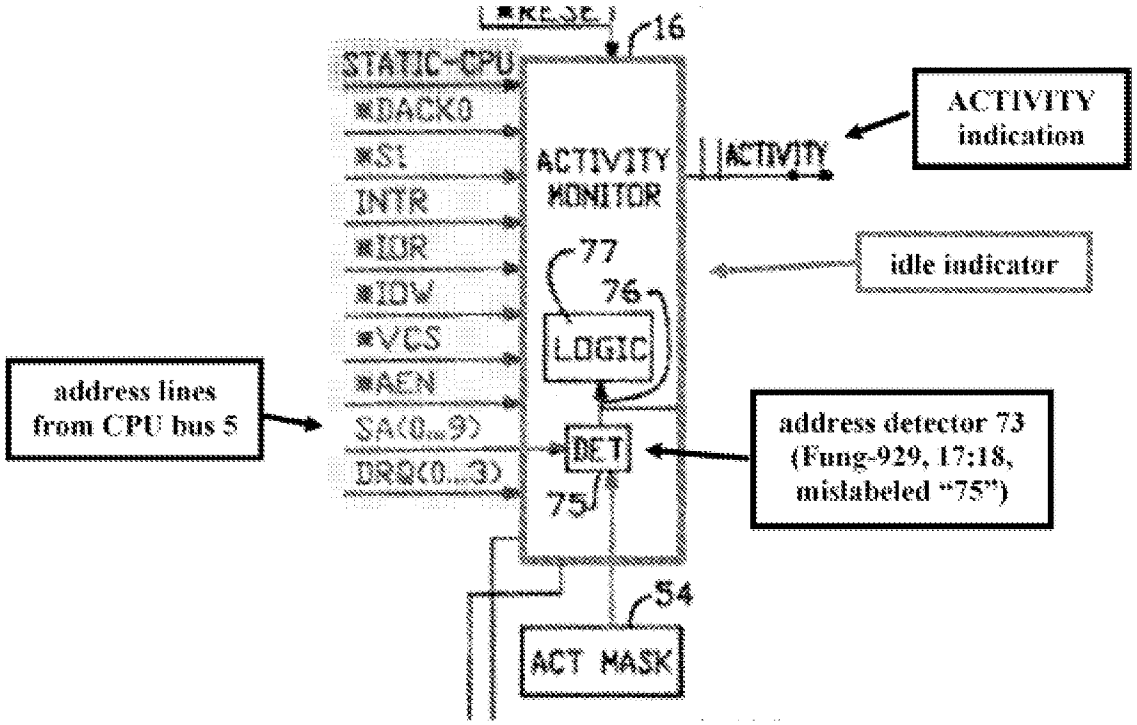


FIG.—2

Fung-929, Fig. 2 (annotated) showing PMU 15 components.

Fung-929 describes activity monitor 16 as coupled to the processor because activity monitor 16 receives signals that originate in the processor including "control lines and address lines SA(O . . . 9) from [CPU] bus 5[]" where the addresses represent "the address activity of the CPU 4." Fung-929, 17:18-30; id., 5:47-51 ("[H]ardware monitor 79 senses predetermined address ranges... and monitors the activity of addresses by the CPU to addresses within these ranges."), 7:18-19 ("hardware monitor 79 senses the activity of addresses on the [CPU] bus 5."), 6:21-24 ("The hardware monitor 79 (using activity monitor 16) analyzes the address activity on the system bus 5 to provide activity information used to control power management."). Figure 3 shows activity monitor 16 signal inputs.



Fung-929, Fig. 3 (annotated, exploded).

Fung-929 explains:

> The activity monitor 16 includes an address detector 73 [mislabeled "75" in Fig. 3] which receives addresses from [CPU] bus 5 representing the address activity of the CPU 4. The address detector 73 receives, for example, control lines and address lines SA(0 . . . 9) from bus 5 for sensing when those addresses are within the predetermined address set.

Fung-929, 17:18-23. Fung-929's reference to "addresses," "address activity," and "address lines" show addresses the CPU sent and received on CPU bus 5. Thus, it shows that "the address activity of CPU 4" meant addresses for lines carrying signals from CPU 4.

(b) "idle indicator receives an indication when the processor is in a first state"

Fung-929's activity monitor 16 "receives an indication" of the CPU being in an idle state and in a busy state, either of which meets the claimed first state.

(i) Idle State

Activity monitor 16 receives an indication that CPU 4 is "idle," e.g., not performing useful work for a user.

First, activity monitor 16 receives a "STATIC-CPU" input. Fung-929, Fig. 3. The "STATIC-CPU" line is connected to the power supply, e.g., Vcc, "if CPU is static." Fung-929, 11:53-55, 12:27. Put differently, when the CPU is "static" the power supply voltage Vcc is asserted on the STATIC-CPU line, e.g., the STATIC-CPU signal is the power supply voltage Vcc.

The CPU being "static" means it is idle because the CPU's clock is stopped. Fung-929 explains, "CLKOUT, as controlled by PMU 15 and control block 49, drives CPU 4. The CLKOUT clock can be stopped for static CPU's, or reduced automatically by a divisor specified in the CLOCK field of control register 53 during DOZE and SLEEP states." Fung-929, 8:1-5, 16:10-13 Thus, "STATIC-CPU" signal is "an indication" of a CPU idle state, e.g., a "first state," because the CPU performs no useful work for a user (e.g., is "idle") when the clock is stopped in the "static" CPU state. Fung-929, 3:26-27, 8:1-3, 16:10-13.

Thus, when the activity monitor 16 receives Vcc asserted on the STATIC-CPU input, that is receiving an indication that the CPU is in an idle state meeting [1A].

Second, Fung-929 explains that a "DOZE state is entered from the ON state when the activity monitor 16 has not detected activity and therefore has not provided the

ACTIVITY signal within the time, T1, specified by the DOZE timer 63." Fung-929, 16:2-5. In other words, "if no data transfers occur within the specified address ranges for predetermined periods of time, then a power conservation mode is entered to conserve power in the computer system." Fung- 929, 2:60-63.

Thus, activity monitor 16 "receives an indication when the processor is in a first state" comprising an "idle" state as used in the '809 patent.

(ii) Busy State

Fung-929's activity monitor 16 also "receives an indication when the processor is in a first state" comprising a "busy" state (e.g., not "idle" state). This provides an alternative basis to meet limitation [1A].

Activity monitor 16 receives a busy indication in two ways:

First, address detector 73 in activity monitor 16 "provides an address detect signal on line 76" when it senses signals on address lines SA(0...9) "representing the address activity of the CPU 4." Fung-929, 17:18-28. Here, the fact that the address detector 73 provides an address detect signal means that the address line SA(0...9) inputs evaluated by address detector 73 provide an indication that the CPU is in a busy state.

Second, logic 77 in activity monitor 16 generates an "ACTIVITY" signal that places PMU 15 in an "ON" state based on inputs including the "address detect signal on line 76." "The ACTIVITY output is an OR function of a programmable selection of different activities specified in the ACTMASK register 54. When active, this output returns the PMU 15 (and the computer system) to the ON state and retriggers the

DOZE timeout timer 63." Fung-929, 17:36- 40; id., 14:21-22 ("The activity monitor ACTIVITY output is the logical OR of all unmasked activity sources."), 15:40-46 (power management unit 15 is placed in an "ON" state "when the activity monitor 16 detects activity with addresses in the predetermined address set."). Here the PMU state "controls the consumption of power by different parts of the computer 3." Fung-929, 7:19-23.

> *'The ON state can... be entered if the hardware monitor 79 detects a predetermined set of address ranges on [CPU] bus 5. For example, the predetermined set of address ranges monitored for power management typically includes all of the I/O address range, that is, the addresses of the I/O controllers 6-0 through 6-n, and the video memory address range for the video memory locations 8 with the memory 11. Of course, other address ranges can be added to or used as the predetermined set for power management. The set of address ranges including the video memory and the I/O address range has been found to provide excellent information for controlling power management.'*

Fung-929, 10:17-28.

This passage referring to activity monitor input signals, notes that I/O, video memory, and memory address signals were indications that CPU 4 was "busy" (not idle) because these were conventionally signals provided by a CPU when it was operating, and an idle CPU or a CPU with a stopped clock would not provide signals on these addresses. A POSA would have understood that a signal indicating a CPU reading or writing to memory was an indication of a busy (non-idle) CPU because a CPU that is reading or writing to memory is not "idle."

It is agreed that the Fung-119 reference does raise a substantial new question of patentability, as proposed in the request, to at least claim 1 of the '809 patent. There is a substantial likelihood that a reasonable Examiner would consider these teachings important in deciding whether or not this claim is patentable.

Accordingly, the Fung-119 reference does raise a substantial new question to at least claim 1, which question has not been decided in a previous examination of the '809 patent nor was there a final holding of invalidity by the Federal Courts regarding the '809 patent.

Neither the Bohac reference nor the Agarwal reference alone raise an SNQ, however when viewed in combination with the Fung-119 reference do raise and SNQ with respect to the following claims: Bohac for claims 6 and 14 and Agarwal for claim 11. Both Bohac and Agarwal are new art that provide new, non-cumulative technological teachings that were not previously considered nor discussed on the record during prosecution of the '809 patent.

35 USC 325(d)

35 USC 325(d) states in part that "[i]n determining whether to institute or order a proceeding under this chapter, chapter 30, or chapter 31, the Director may take into account whether, and reject the petition or request because, the same or substantially

the same prior art or arguments previously were presented to the Office.". Thus, in order for the Director to exercise discretion as to whether to Order a reexamination proceeding under chapter 30, the request must first be determined to be based on the same or substantially the same prior art or arguments that previously were presented to the Office.

A review of the Office post grant history for the '809 Patent, indicates that the patent has been the subject of a single prior Office post grant challenge.

On July 5, 2022 petitioner Google, LLC, filed a petition seeking *inter partes* review of claims 1-17 of the '809 patent (IPR2022-01197), which asserted the following grounds as raising a reasonable likelihood in prevailing (RLP):

RLP	Claims Challenged	35 USC §	References
1	1–3, 5, 7, 9–10, 13, 15–17	102/103(a)	Ogawa
2	6,14	103(a)	Ogawa, Bohac
3	6,14	103(a)	Ogawa, McAnlis
4	10,12	103(a)	Ogawa, Zalewski and/or Ogawa, Cellular-IRIX
5	11	103(a)	Ogawa, Zalewski, McAnlis and/or Ogawa, Cellular-IRIX, McAnlis
6	1,2,4,7–11,13 15–17	103(a)	Vea
7	6, 14	103(a)	Vea, Bohac
8	10, 12	103(a)	Vea, Zalewski and/or Vea, Cellular-IRIX

On January 3, 2023, the Patent Trial and Appeal Board (PTAB) issued a decision discretionarily refusing to institute *inter partes* review under both 35 USC 314(a) and 35 USC 325(d). In the PTAB's decision, the decision held that with regard to grounds 1-5 based on the Ogawa reference, failed to demonstrate that Ogawa taught or suggested "an idle indicator . . . [which] receives an indication when the processor is in a first state" recited in independent claim 1 and failed to demonstrate that Ogawa taught or suggested "providing a busy indication to a counter associated with a busy processor" as recited in independent claim 13. Thus, the Board held the petition failed to raise and

RLP with respect to grounds 1-5. With respect asserted RLP grounds 6-8, the PTAB discreationary denied reexamination under 325(d), based on the PTAB's conclusion that a European counterpart to the Vea reference was evaluated after allowance, by the Examiner initialing next to it on a 1449 during the original prosecution of the '809 patent.

A comparison between the prior art and augments presented in the prior denied *inter partes* review petition and the current reexamination request for reexamination of the '809 patent, indicates that the prior art and arguments are not the same or substantially the same as the art/arguments previously presented to the Office. As stated above, the current Request asserts the following grounds as raising a substantial new question of patentability (SNQ) to the claims of the '809 patent.

SNQ	Claims Challenged	35 USC §	References
1	1, 2, 5, 9, 10, 13, 15, 17	103(a)	Theimer, Ogawa
2	6, 14	103(a)	Theimer, Ogawa, Bohac
3	11	103(a)	Theimer, Ogawa, McAnlis
4	1, 2, 5, 9, 10, 13, 15, 17	103(a)	Hoekstra, Ogawa
5	6, 14	103(a)	Hoekstra, Ogawa, Bohac
6	11	103(a)	Hoekstra, Ogawa, McAnlis
7	1, 8-12	102	Fung-119
8	2-5, 13, 15, 17	103(a)	Fung-119
9	6, 14	103(a)	Fung-119, Bohac
10	7, 16	103(a)	Fung-119, Argawal

As an initial matter, none of the grounds presented in the current reexamination request are based on the identical art combinations presented in the prior denied petition. Further, neither the Vea reference or one of its counterparts were presented in this reexamination request. In addition, while the Ogawa, McAnlis and Bohac references were presented in the prior reexam request, they are presented only a secondary references for dependent claims of the '809 patent. Therefore, the art and arguments are not the same as the art and arguments previously presented to the Office.

Further, As stated above, newly present Theimer, Hoekstra and Fung-119 (which incorporates by reference Fung-929) are cited as disclosing the claimed limitation of an "idle indicator coupled to a processor, wherein the idle indicator receives an indication when the processor is in a first state". Thus, since the newly presented prior art combination asserted as raising an SNQ, discloses the very teachings held to be deficient from the prior art combinations presented in the prior denied IPR petition, and because neither Vea or a counterpart to Vea were presented in this Request, the prior art and arguments in the 90/019,429 Request are also not substantially the same as the art/arguments previously presented to the Office.

Thus, because both the prior art grounds and arguments presented in the instant Request are neither the same nor substantially the same as those previously presented to the Office, the statutory threshold pursuant to 35 USC 325(d) to permit the Director to exercise to discretion to reject the instant reexamination request is not met.

Accordingly, *ex parte* reexamination is Ordered based on the findings above that the request raises a substantial new question of patentability of claims 1-17 of the '809 patent.

Summary

Claims 1-17 are hereby ORDERED to be reexamined.

Claims 18-20 are not subject to reexamination.

Conclusion

Extensions of time under 37 CFR 1.136(a) do not apply in reexamination proceedings. The provisions of 37 CFR 1.136 apply only to "an applicant" and not to

parties in a reexamination proceeding. Further, in 35 U.S.C. 305 and in 37 CFR 1.550(a), it is required that reexamination proceedings "will be conducted with special dispatch within the Office."

The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the patent throughout the course of this reexamination proceeding. The requester is also reminded of the ability to similarly appraise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP § § 2207, 2282, and 2286.

All correspondence relating to this *ex parte* reexamination proceeding should be directed:

By Mail to: Mail Stop Ex Parte Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Electronically: Registered users may submit via Patent Center at:
https://patentcenter.uspto.gov.

For electronic transmissions, 37 CFR 1.8(a)(1)(i)(C) and (11) states that correspondence (except for a request for reexamination and a corrected or replacement request for reexamination) will be considered timely filed if (a) it is transmitted via the USPTO patent electronic filing system in accordance with 37 CFR 1.6(a)(4), and (b) includes a certificate of transmission for each piece of correspondence stating the date of transmission, which is prior to the expiration of the set period of time in the Office action.

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

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